

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S12 0	2274	((multiple plural\$3) same counter and (add\$3 increment\$3)).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 13:29
S11 1	53	(node same (processor cpu) same counter and (add\$3 increment\$3)).bsum.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 13:29
S12 2	12	("4833629").URPN.	USPAT	OR	ON	2007/05/15 13:57
S12 1	286	((hardware computer processor cpu) same (multiple plural\$3) same counter same (add\$3 increment\$3)).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 14:03
S12 3	58	(event same (multiple plural\$3) same counter same (add\$3 increment\$3)).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 14:04
S12 4	2	("6097781"   "6314155").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/15 14:19
S12 5	0	377/26.ccls. and @pd>"20070228"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 15:11
S11 5	101	377/26.ccls. and (multiple plurality).bsum.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 15:14

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S12 8	147	708/672.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 15:32
S12 7	252	708/670.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 15:32
S12 6	34	"377"/\$.ccls. and ((multiple plurality) with (incrementer adder)).bsum.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 15:32
S12 9	77	708/672.ccls. and counter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 15:33
S13 0	33	708/672.ccls. and (multiple purality)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/15 15:34
S13 1	42	memory near array with counter same (incrementer adder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 08:16
S13 3	861	"377"/\$.ccls. and (multiple plurality) with (add\$3 increment\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 08:37

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S13 2	4495	"377"/\$.ccls. and (multiple plurality) with (add\$3 increment\$3 count\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 08:37
S13 4	73	"377"/\$.ccls. and ((multiple plurality) with (add\$3 increment\$3)).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 08:54
S13 6	313	"377"/49.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 09:01
S13 5	248	"377"/37.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 09:01
S13 7	3	("4575864"   "4860357"   "4939683").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/16 09:15
S13 8	5	((("5410721") or ("6038660") or ("20040225734") or ("6701447") or ("5835705"))).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/05/16 09:17
S14 0	380	program adj counter same incrementer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 09:22
S13 9	2	("6038660").URPN.	USPAT	OR	ON	2007/05/16 09:22

## EAST Search History

S14 1	42	(program adj counter same incrementer).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 09:30
S14 3	211	((multiple plurality) with event same counter).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 09:31
S14 2	0	((multiple plurality) with event same counter same incrementer).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 09:31
S14 6	2	("6898179").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/16 09:39
S14 5	3	("6718403").URPN.	USPAT	OR	ON	2007/05/16 09:39
S14 7	1	("6658584").URPN.	USPAT	OR	ON	2007/05/16 09:41
S14 8	11	("5414704"   "5446560"   "5471640"   "5615135"   "5687173"   "5784554"   "5790625"   "5991708"   "6052708"   "6360337"   "6519330").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/16 09:43
S14 4	44	((multiple plurality) near event same counter).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 09:59

## EAST Search History

S14 9	17	((multiple plurality) same performance near counter).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 10:08
S15 1	2	(performance near counter).ab. and incrementer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 10:10
S15 0	175	(performance near counter).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 10:10
S15 3	25	(event near counter).ab. and (incrementer adder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 10:14
S15 2	15	(performance near counter).ab. and (incrementer adder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 10:14
S15 4	22	("3589474"   "3748451"   "4034353"   "4231106"   "4676077"   "5003248"   "5097490"   "5167033"   "5343461"   "5426741"   "5493673"   "5615135"   "5646553"   "5699348"   "5773994"   "5838688"   "6044400"   "6065130"   "6194918"   "6353920"   "6360335"   "6415363").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/16 10:49
S15 5	1	("6785851").URPN.	USPAT	OR	ON	2007/05/16 10:50

## EAST Search History

L4	3	(counter same index same incrementer).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/16 13:30
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memory array multiple counter

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## Patents

Patents 1 - 10 on memory array multiple counter. (0.33 seconds)

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### Multiple bank memory with auto refresh to specified bank

US Pat. 5627791 - Filed Feb 16, 1996 - Micron Technology, Inc.

The **memory** device of claim 3 wherein the one of the refreshing of the bank 0**memory array** while an active and **multiple bank memory** arrays is predetermined ...

### Network communications adapter with dual interleaved memory banks servicing multiple processors

US Pat. 4933846 - Filed Apr 24, 1987 - Network Systems Corporation

Timer 218 is a 32-bit **counter** clocked ... 1, the Central **Memory** 100 is composedof 1 to 4 identical **memory array** boards. Each **memory array** board 65 contains ...

### Database sort and merge apparatus with multiple memory arrays having alternating access

US Pat. 5210870 - Filed Mar 27, 1990 - International Business Machines

The i and j pointers, generated respectively by the i **counter** 722 and the j**counter** 724, provide addressing for the source **array**. ...

### Separately addressable memory arrays in a multiple array semiconductor chip

US Pat. 4636986 - Filed Jan 22, 1985 - Texas Instruments Incorporated

If only one pixel mapped **memory array** were utilized, it would require ...A **counter** (not shown) counts the number of shift clocks to provide a count output ...

### Non-volatile memory system

US Pat. 4503494 - Filed Jun 26, 1980 - Texas Instruments Incorporated

Alternatively, the **memory array** 10 636 may be comprised of an **array** organized... **counter** 634, the **memory** 624 outputs data from **multiple memory** locations, ...

### First-in, first-out memory with counter address pointers for generating multiple memory status flags

US Pat. 4864543 - Filed Apr 30, 1987 - Texas Instruments Incorporated

isb shows a higher-order ring **counter** comparator indicated generally at 420. ...The illustrated embodiment, of course, is provided for a **memory array** of 64 ...

### Content addressable memory array with priority encoder

US Pat. 4928260 - Filed May 11, 1988 - Advanced Micro Devices, Inc.

Op Code 15 Load Segment **Counter** User can change the segment **counter** to get to... Under the **multiple** match condition in which there are more than 1 match ...

### Read/write memory having a multiple column select mode

US Pat. 4807189 - Filed Aug 5, 1987 - Texas Instruments Incorporated

Sa illustrates a timing diagram of a **memory** cordingly, toggle **counter**/decoder 22

receives the cycle for loading the write mask register during the 40....

### Method and apparatus for execution of operations in a flash memory array

US Pat. 5509134 - Filed Jun 30, 1993 - Intel Corporation

... wherein said **array** controller further comprises a program **counter** which points... **memory** system, to utilize the same code, thereby supporting **multiple** ...

### Memory system having a common interface

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multiple counter incrementer OR adder

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## Patents

Patents 1 - 10 on multiple counter incrementer OR adder. (0.24 seconds)

Did you mean: **multiple counter increment OR adder**

### Multiple instruction set mapping

US Pat. 5568646 - Filed Sep 19, 1994 - Advanced Risc Machines Limited

A program **counter** register 22, which is part of the processor core 2, is shown addressing the memory system 4. A program **counter incrementer** 24 serves to ...

### Data processing with multiple instruction sets

US Pat. 5740461 - Filed Oct 22, 1996 - Advanced RISC Machines Limited

A program **counter incrementer** 24 serves to instructions. This decoding means 30 decodes the first increment the program **counter** value within the program ...

### Method and apparatus for selectively encoding and decoding a digital motion video signal at ...

US Pat. 5122873 - Filed Feb 19, 1991 - Intel Corporation

Recall that all the D coordinates X, Y are applied to an address **counter** ...  
offset DPCM data from variable length decoder (FIG. **adder** 5406 and added to the ...

### Method and circuitry for symbol timing and frequency offset estimation in time division multiple ...

US Pat. 4941155 - Filed Nov 16, 1989 - Bell Communications Research, Inc.

In accordance with the count of **counter** 407, the values stored 16 this ...  
The output of digital **adder** 422 is input to subtracter 423 and a register 424 ...

### Pseudorandom noise ranging receiver which compensates for multipath distortion by making use of ...

US Pat. 5414729 - Filed Nov 29, 1993 - NovAtel Communications Ltd.

As shown, an **adder** 223 is arranged to add the contents of the Doppler register  
... The chip **counter** 2266 is used to determine the duration of a complete PRN ...

### Data processing device with multiple on chip memory buses

US Pat. 4912636 - Filed Mar 13, 1987

4, program **counter** control logic 204 contains an **adder** 203 which receives the contents of program **counter** 92. Control logic 202 (preferably combinatorial ...

### Electronic pitch detection for musical instruments

US Pat. 4351216 - Filed Aug 22, 1979

When **adder** 974 in addition to the all zeros word and the transmitted through and  
... The **multiple counter** comprises a flip-flop to be set, so that the Q bar ...

### System for displaying character and graphic information on a color video display with unique ...

US Pat. 4180805 - Filed Apr 6, 1977 - Texas Instruments Incorporated

The ROM word address is a six-bit address produced in a program **counter** 36 ...  
The input to 60 the **adder** 50 is determined by an input selector 51 which ...

### Machine for multiple instruction execution

US Pat. 4295193 - Filed Jun 29, 1979 - International Business Machines Corporation

The gate 380 for updating the instruction **counter** 362 at active state of line  
... via a cable 394 to an **adder** 396 for addition with as previously described, ...